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transistor when the desired output of said emitter follower is a preselected logic level.

2. The apparatus of Claim 1 further comprising a third transistor, the input terminal of which is coupled to receive said drive signal, said third transistor connecting the output of said emitter follower to a preselected voltage when the desired output of said emitter follower is said preselected logic level.

3. The apparatus of Claim 1, further comprising a second buffer circuit operatively coupling the said one output of said pre-amplifier to said output buffer.

4. Apparatus for converting low level input signals to CMOS level signals, said apparatus comprising:

(a) a pre-amplifier coupled to receive said low level input signals and for producing two output signals, said two output signals being at opposite logic levels,

(b) first and second output buffers each operatively coupled to receive a different of said two output signals, each of said first and second output buffers having an emitter follower transistor, with the load of said emitter follower transistor provided by a second transistor, and

(c) a circuit for providing different drive signals for each of said second transistors, each said drive signal serving to turn off one of said second transistors when the desired output of the corresponding emitter follower is a preselected logic level.

5. The apparatus of Claim 4 further comprising a pair of third transistors, each of said pair of third transistors being associated with the emitter follower of one of said first and second output buffers and having an input terminal coupled to receive the drive signal for the second transistor of its associated emitter follower, said third transistor connecting the output of its

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associated emitter follower to a preselected voltage when the desired output of the associated emitter follower is said preselected logic level.

6. The apparatus of Claim 4, further comprising intermediate buffer circuits, the first operatively coupling a first output of said pre-amplifier to said first output buffer and the second

5 operatively coupling a second output of said pre-amplifier to said second output buffer.

Sub A37 7. A method for converting low level input signals to CMOS level output signals, said method comprising the steps of:

(a) applying said low level input signals to a pre-amplifier,

(b) operatively coupling a first output of said pre-amplifier to an output buffer, said
10 output buffer having a first transistor in an emitter follower configuration, with the load of said emitter follower provided by a second transistor, and

(c) generating a drive signal, said drive signal serving to turn off said second transistor

when the desired output of said emitter follower is a preselected logic level.

8. The method of Claim 7 comprising the further step of applying said drive signal to a

15 third transistor, said third transistor connecting the output of said emitter follower to a preselected voltage when the desired output of said emitter follower is said preselected logic level.

9. The method of Claim 7 comprising the further step of applying said first output of said pre-amplifier to an intermediate buffer circuit and applying the output of said buffer circuit to said output buffer.